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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,295	YOSHIDA, DAISUKE	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/505,194.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *18 April 2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent ***Application No. 09/505,194*** (now ***Patent No. 6,670,938***), filed on ***16 February 2000***.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "***MEMO-CLK***" (e.g., see Fig. 1); "***7***" (e.g., see Fig. 2); "***25***" (e.g., see Fig. 10). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

4. The disclosure is objected to because of the following informalities: The phrase, "***in in columns***" should be change, for example to, "***in columns***" (see Page 8, Line 13).

Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 8-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a plurality of signal lines***" (in line 3); "***a first common signal line***" (in line 10); "***a second common signal line***" (in line 12); "***a signal line***" (in line 15); and "***the signal line***" (in line 19).

It would be unclear to one having ordinary skill in the art whether the "***first and second common signal lines***" are common elements of the earlier established "***plurality of signal lines***"; or rather whether the "***first and second common signal lines***" are distinct and independent from the earlier established "***plurality of signal lines***".

Also, it would be unclear to one having ordinary skill in the art whether "***a/the signal line***" is a common element of the earlier established "***plurality of signal lines***"; whether the "***a/the signal line***" is a common element of the earlier established "***first and/or second common signal lines***"; or rather whether the "***a/the signal line***" is distinct and independent from all the other earlier established "***signal lines***".

An omitted structural cooperative relationship results from the claimed subject matter: "***supplying picture signals***" (in line 5); "***supplying picture signals of one polarity***" (in line 11); "***supplying picture signals of the other polarity***" (in line 13); and "***the picture signals of one polarity***" (in line 16).

It would be unclear to one having ordinary skill in the art whether the "***picture signals of one polarity***" are common elements of the earlier established "***picture signals***"; or rather whether

the "***picture signals of one polarity***" are distinct and independent from the earlier established "***picture signals***".

Similarly, it would be unclear to one having ordinary skill in the art whether the "***picture signals of the other polarity***" are common elements of the earlier established "***picture signals***"; or rather whether the "***picture signals of the other polarity***" are distinct and independent from the earlier established "***picture signals***".

Also, it would be unclear to one having ordinary skill in the art whether "***the picture signals of one polarity***" refers back to only the earlier established "***picture signals of one polarity***"; or rather whether the "***the picture signals of one polarity***" also refers back to the earlier established "***picture signals of the other polarity***".

9. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a plurality of signal lines***" (in line 3); "***a first common signal line***" (in line 10); "***a second common signal line***" (in line 12); "***a signal line***" (in line 15); and "***a signal line***" (in line 19).

It would be unclear to one having ordinary skill in the art whether the "***first and second common signal lines***" are common elements of the earlier established "***plurality of signal lines***"; or rather whether the "***first and second common signal lines***" are distinct and independent from the earlier established "***plurality of signal lines***".

Also, it would be unclear to one having ordinary skill in the art whether each instance of "***a signal line***" is a common element of the earlier established "***plurality of signal lines***"; whether each instance of "***a signal line***" is a common element of the earlier established "***first and/or second common signal lines***"; whether each instance of "***a signal line***" refers to the same identical one "***signal line***"; or rather whether each instance of "***a signal line***" is distinct and independent from all the other earlier established "***signal lines***".

An omitted structural cooperative relationship results from the claimed subject matter: "***supply picture signals***" (in line 5); "***supplying picture signals of one polarity***" (in line 11); "***supplying picture signals of the other polarity***" (in line 13); "***the picture signals of one polarity***" (in line 16); and "***picture signals of the other polarity***" (in line 19).

It would be unclear to one having ordinary skill in the art whether the "***picture signals of one polarity***" are common elements of the earlier established "***picture signals***"; or rather whether the "***picture signals of one polarity***" are distinct and independent from the earlier established "***picture signals***".

Similarly, it would be unclear to one having ordinary skill in the art whether the "***picture signals of the other polarity***" are common elements of the earlier established "***picture signals***"; or rather whether the "***picture signals of the other polarity***" are distinct and independent from the earlier established "***picture signals***".

Also, it would be unclear to one having ordinary skill in the art whether "***the picture signals of one polarity***" refers back to only the earlier established "***picture signals of one polarity***"; or rather whether the "***the picture signals of one polarity***" also refers back to the earlier established "***picture signals of the other polarity***".

10. Claims 10-15 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***A liquid crystal apparatus***" (in line 1 of each claim). It would be unclear to an artisan whether each of the dependent claims is referring to the identical "***liquid crystal apparatus***" claimed in the respective independent claim; or rather whether each of the dependent claims is referring a "***liquid crystal apparatus***" distinct and independent from the "***liquid crystal apparatus***" of the respective independent claims.

11. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a transistor***" (in line 2) and "***a transistor***" (in line 3). It would be unclear to an artisan whether a single identical "***transistor***" is being claimed; or rather whether plural distinct and independent "***transistors***" are being claimed.

12. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***picture signal-supplying means***" (in claim 11, line 2); "***first and second picture signal-generating means***" (in claim 11, line 3); "***positive-polarity picture signals***" (in claim 11, line 3); "***negative-polarity picture signals***" (in claim 11, line 4); "***generates picture signals***" (in claim 11, line 5); "***generates picture signals***" (in claim 11, line 7); "***the picture signal-generating means***" (in claim 11, line 13); "***supplying picture signals***" (in claim 8, line 5); "***supplying picture signals of one polarity***" (in claim 8, line 11); "***supplying picture signals of the other polarity***" (in claim 8, line 13); "***the picture signals of one polarity***" (in claim 8, line 16).

It would be extremely unclear to one having ordinary skill in the art what relationship (if any) exists between all the above "***picture signal***" limitations.

Additionally, it would be unclear to one having ordinary skill in the art whether "***the picture signal-generating means***" refers to the "***first picture signal-generating means***"; or rather whether "***the picture signal-generating means***" refers to the "***second picture signal-generating means***".

13. Claim 11 recites the limitation "***the picture signal-generating means***" (in line 13). There is insufficient antecedent basis for this limitation in the claim.

14. Claim 12 recites the limitation "***the range***" (in line 2). There is insufficient antecedent basis for this limitation in the claim.

15. Claim 13 recites the limitation "***picture signal-supplying means***" (in line 2). There is insufficient antecedent basis for this limitation in the claim.

16. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a common substrate with the active matrix substrate***" (in line 3). It would be unclear to an artisan whether a single identical "***substrate***" is being claimed; or rather whether plural distinct and independent "***substrates***" are being claimed.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims 8-15 are rejected under 35 U.S.C. 102(e) as being anticipated by ***Hiroki (US 6,628,253 B1)***.

Regarding claim 8, Hiroki discloses a liquid crystal apparatus, comprising:

a liquid crystal device [Fig. 7; 1] comprising an active matrix substrate (see Fig. 8; Column 1, Lines 8-15) having thereon a plurality of signal lines [Fig. 8A; Signal Lines] arranged in columns, a plurality of scanning lines [Fig. 7; Scan Lines] arranged in rows, and pixel electrodes [Fig. 8A; A, B, C] each connected via a pixel switch [Fig. 8A; thin film transistors] to an intersection of the signal lines and the scanning lines so as to supply picture signals [Fig. 8A; Analog Video Signals] to the pixel electrodes via the signal lines, a counter substrate disposed opposite to the active matrix substrate, and a liquid crystal disposed between the active matrix substrate and the counter substrate (see Column 6, Line 63 - Column 7, Line 6), and

drive means [Fig. 7; 5] for driving the liquid crystal device, wherein said drive means includes:

a first common signal line [Fig. 8A; horizontal signal line segment output from 27] for supplying picture signals of one polarity [e.g., positive polarity] to each of the plurality of signal lines (see Figs. 10-12; Column 3, Line 4 -Column 4, Line 65),

a second common signal line [Fig. 8A; the vertical signal line segments between the transfer switches and the horizontal signal line segment output from 27] for supplying picture signals of the other polarity [e.g., negative polarity] to each of the plurality of signal lines (wherein Hiroki teaches reversing picture signal polarity between pixels, columns, rows, and/or frames),

a first transfer switch [Fig. 8A; positive-signal controlled leftmost CMOS circuit within the 'Sampling Circuit and Buffer Circuit'] for connecting (electrically) a signal line [Fig. 8A; Signal Line(1)] with the first common signal line for selectively supplying the picture signals of one polarity to the signal line, and

a second transfer switch [Fig. 8A; negative-signal controlled leftmost CMOS circuit within the 'Sampling Circuit and Buffer Circuit'] for connecting (electrically) the signal line [Fig. 8A; Signal Line(1)] with the second common signal line for selectively supplying the picture signals of other polarity to the signal line, wherein the signal line is connected to the first transfer switch and the second transfer switch (see Fig. 8A), and

column inversion [Figs. 11A, 11B, 11C] drive means for:

in a first frame [Fig. 10; '1 Frame'], selectively turning on the first transfer switch for the signal line, and

in a second frame [Fig. 10; 'Next Frame'], selectively turning on the second transfer switch for the signal line (see Column 3, Line 4 -Column 4, Line 65).

Regarding claim 9, this claim is rejected by the reasoning applied in rejecting claim 8; furthermore, Hiroki discloses

a liquid crystal device [Fig. 7; 1] comprising an active matrix substrate (see Fig. 8; Column 1, Lines 8-15) having thereon a plurality of signal lines [Fig. 8A; Signal Lines] arranged in columns, a plurality of scanning lines [Fig. 7; Scan Lines] arranged in rows, and pixel electrodes [Fig. 8A; A, B, C] each connected via a pixel switch [Fig. 8A; thin film transistors] to an intersection of the signal lines and the scanning lines so as to supply picture signals [Fig. 8A; Analog Video Signals] to the pixel electrodes via the signal lines, a counter substrate disposed opposite to the active matrix substrate, and a liquid crystal disposed between the active matrix substrate and the counter substrate (see Column 6, Line 63 - Column 7, Line 6), and

drive means [Fig. 7; 5] for driving the liquid crystal device, wherein said drive means includes:

a first common signal line [Fig. 8A; horizontal signal line segment output from 27] for supplying the picture signals of one polarity [e.g., positive polarity] to each of the plurality of signal lines (see Figs. 10-12; Column 3, Line 4 -Column 4, Line 65),

a second common signal line [Fig. 8A; the vertical signal line segments between the transfer switches and the horizontal signal line segment output from 27] for supplying picture signals of the other polarity [e.g., negative polarity] to each of the plurality of signal lines (wherein Hiroki teaches reversing picture signal polarity between pixels, columns, rows, and/or frames),

a first transfer switch [Fig. 8A; positive-signal controlled leftmost CMOS circuit within the 'Sampling Circuit and Buffer Circuit'] for connecting (electrically) a signal line [Fig. 8A; Signal Line(1)] with the first common signal line for selectively supplying the picture signals of one polarity to the signal line, and

a second transfer switch [Fig. 8A; negative-signal controlled leftmost CMOS circuit within the 'Sampling Circuit and Buffer Circuit'] for connecting (electrically) a signal line [Fig. 8A; Signal Line(1)] with the second common signal line for selectively supplying picture signals of other polarity to the signal line, wherein the signal line is connected to the first transfer switch and the second transfer switch (see Fig. 8A), and

a dot inversion [Fig. 12C] drive means for:

in a first frame [Fig. 10; '1 Frame'], selectively turning on the first transfer switch for the signal line at a first timing, and selectively turning on the second transfer switch for the signal

line at a second timing different from the first timing (wherein the second inverter within the 'Sampling Circuit and Buffer Circuit' will inherently delay the control signal fed to the right side of the CMOS circuit, compared to the non-inverted control signal fed to the left side of the CMOS circuit); and

in a second frame [Fig. 10; 'Next Frame'], selectively turning on the second transfer switch for the signal line at a third timing, and selectively turning on the first transfer switch for the signal line at a fourth timing different from the third timing (see Column 3, Line 4 -Column 4, Line 65 -- wherein, again, the second inverter within the 'Sampling Circuit and Buffer Circuit' will inherently delay the control signal fed to the right side of the CMOS circuit, compared to the non-inverted control signal fed to the left side of the CMOS circuit).

Regarding claim 10, Hiroki discloses the first transfer switch comprises a transistor of a first conductivity type and the second transfer switch comprises a transistor of a second conductivity type different from the first conductivity type (see Fig. 8A; Column 3, Lines 4-46 -- in particular, see the CMOS circuitry within the 'Sampling Circuit and Buffer Circuit').

Regarding claim 11, Hiroki discloses picture signal supply means including first and second picture signal-generating means [Fig. 10; 22] for generating positive-polarity picture signals [Fig. 10; Positive Analog Video Signal 27] and negative-polarity picture signals [Fig. 10; Negative Analog Video Signal 27], respectively, supplied to the first and second common signal lines, respectively; wherein the first picture signal generating means generates picture signals in a range between a highest voltage and a central voltage supplied to the pixel electrodes (see Fig.

10); the second picture signal-generating means generates picture signals in a range between the central voltage and a lowest voltage supplied to the pixel electrodes (see Fig. 10); the first and second picture signal-generating means are operated at different supply voltages (see Fig. 10); the supply voltages for the first picture signal-generating means are set to be the highest voltage + α and the central voltage - α; and the supply voltages for the second picture signal-generating means are set to be the central voltage + α and the lowest voltage - α, wherein α denotes α voltage lowering margin due to an internal resistance in the picture signal-generating means (see Column 3, Line 4 -Column 4, Line 65).

Regarding claim 12, Hiroki discloses α is in the range of 0 volt to 1 volt (see Fig. 12; Column 3, Line 4 -Column 4, Line 65).

Regarding claim 13, Hiroki discloses the first and second transfer switches and the picture signal supply means are disposed on a common substrate with the active matrix substrate (see Fig. 7; Column 1, Line 14 - Column 3, Line 3).

Regarding claim 14, Hiroki discloses the active matrix substrate comprises an insulating substrate (see Column 8, Lines 25-41).

Regarding claim 15, Hiroki discloses the active matrix substrate comprises a single crystal substrate (see Column 8, Lines 25-41).

19. Claims 8-15 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Takahara et al (US 5,436,635 A)***.

Regarding claim 8, Takahara discloses a liquid crystal apparatus (see the Abstract), comprising:

a liquid crystal device (see Column 1, Lines 5-16) comprising an active matrix (see claim 3) substrate [Fig. 13; 31] having thereon a plurality of signal lines [Fig. 11; S] arranged in columns, a plurality of scanning lines [Fig. 11; G] arranged in rows, and pixel electrodes [Fig. 11; p] each connected via a pixel switch [Fig. 11; T] to an intersection of the signal lines and the scanning lines so as to supply picture signals [Fig. 11; V] to the pixel electrodes via the signal lines, a counter substrate [Fig. 13; 32] disposed opposite to the active matrix substrate, and a liquid crystal [Fig. 13; 37] disposed between the active matrix substrate and the counter substrate (see Column 9, Line 11 - Column 10, Line 21), and

drive means [Fig. 11; 11, 12, 71] for driving the liquid crystal device, wherein said drive means includes:

a first common signal line [Fig. 11; V(P)] for supplying picture signals of one polarity [Fig. 11; V+] to each of the plurality of signal lines,

a second common signal line [Fig. 11; V(M)] for supplying picture signals of the other polarity [Fig. 11; V-] to each of the plurality of signal lines (see Column 21, Lines 3-56),

a first transfer switch [Fig. 11; SW_{p1}] for connecting a signal line [Fig. 11; S1] with the first common signal line for selectively supplying the picture signals of one polarity to the signal line, and

a second transfer switch [Fig. 11; SW_{m1}] for connecting the signal line [Fig. 11; S1] with the second common signal line for selectively supplying the picture signals of other polarity to the signal line, wherein the signal line is connected to the first transfer switch and the second transfer switch (see Fig. 11), and

column inversion drive means [Fig. 11; a, 123, b] for:

in a first frame, selectively turning on the first transfer switch for the signal line, and

in a second frame, selectively turning on the second transfer switch for the signal line (see Figs. 11 & 12; Column 20, Line 24 - Column 21, Line 56).

Regarding claim 9, this claim is rejected by the reasoning applied in rejecting claim 8; furthermore, Takahara discloses a liquid crystal apparatus (see the Abstract), comprising:

a liquid crystal device (see Column 1, Lines 5-16) comprising an active matrix (see claim 3) substrate [Fig. 13; 31] having thereon a plurality of signal lines [Fig. 11; S] arranged in columns, a plurality of scanning lines [Fig. 11; G] arranged in rows, and pixel electrodes [Fig. 11; p] each connected via a pixel switch [Fig. 11; T] to an intersection of the signal lines and the scanning lines so as to supply picture signals [Fig. 11; V] to the pixel electrodes via the signal lines, a counter substrate [Fig. 13; 32] disposed opposite to the active matrix substrate, and a liquid crystal [Fig. 13; 37] disposed between the active matrix substrate and the counter substrate (see Column 9, Line 11 - Column 10, Line 21), and

drive means [Fig. 11; 11, 12, 71] for driving the liquid crystal device, wherein said drive means includes:

a first common signal line [Fig. 11; V(P)] for supplying picture signals of one polarity [Fig. 11; V+] to each of the plurality of signal lines,

a second common signal line [Fig. 11; V(M)] for supplying picture signals of the other polarity [Fig. 11; V-] to each of the plurality of signal lines (see Column 21, Lines 3-56),

a first transfer switch [Fig. 11; SW_{p1}] for connecting a signal line [Fig. 11; S1] with the first common signal line for selectively supplying the picture signals of one polarity to the signal line, and

a second transfer switch [Fig. 11; SW_{m1}] for connecting the signal line [Fig. 11; S1] with the second common signal line for selectively supplying the picture signals of other polarity to the signal line, wherein the signal line is connected to the first transfer switch and the second transfer switch (see Fig. 11), and

a dot inversion [Fig. 11; a, 123, b] drive means for:

in a first frame, selectively turning on the first transfer switch for the signal line at a first timing, and selectively turning on the second transfer switch for the signal line at a second timing different from the first timing; and

in a second frame, selectively turning on the second transfer switch for the signal line at a third timing, and selectively turning on the first transfer switch for the signal line at a fourth timing different from the third timing (see Figs. 11 & 12; Column 20, Line 24 - Column 21, Line 56).

Regarding claim 10, Takahara discloses the first transfer switch comprises a transistor (see Column 6, Lines 52-65) of a first conductivity type and the second transfer switch comprises

a transistor of a second conductivity type different from the first conductivity type (see Column 21, Lines 5-56).

Regarding claim 11, Takahara discloses picture signal supply means including first [Fig. 11; V(P)] and second picture signal-generating means [Fig. 11; V(M)] for generating positive-polarity picture signals [Fig. 11; V+] and negative-polarity picture signals [Fig. 11; V-], respectively, supplied to the first and second common signal lines, respectively; wherein the first picture signal generating means generates picture signals in a range between a highest voltage and a central voltage supplied to the pixel electrodes; the second picture signal-generating means generates picture signals in a range between the central voltage and a lowest voltage supplied to the pixel electrodes; the first and second picture signal-generating means are operated at different supply voltages; the supply voltages for the first picture signal-generating means are set to be the highest voltage + α and the central voltage - α; and the supply voltages for the second picture signal-generating means are set to be the central voltage + α and the lowest voltage - α, wherein α denotes α voltage lowering margin due to an internal resistance in the picture signal-generating means (see Figs. 11 & 12; Column 20, Line 24 - Column 21, Line 56).

Regarding claim 12, Takahara discloses α is in the range of 0 volt to 1 volt (see Figs. 11 & 12; Column 20, Line 24 - Column 21, Line 56).

Regarding claim 13, Takahara discloses the first and second transfer switches and the picture signal supply means are disposed on a common substrate with the active matrix substrate (see Figs. 11 & 12; Column 20, Line 24 - Column 21, Line 56 and Column 13, Lines 20-35).

Regarding claim 14, Takahara discloses the active matrix substrate comprises an insulating substrate (see Column 8, Lines 25-41 and Column 13, Lines 20-35).

Regarding claim 15, Takahara discloses the active matrix substrate comprises a single crystal substrate (see Column 9, Line 10 - Column 13, Line 65).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 10, 13, and 15 are further rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takahara et al (US 5,436,635 A)***.

Regarding claim 10, Takahara discloses the first transfer switch comprises a transistor (see Column 6, Lines 52-65) of a first conductivity type and the second transfer switch comprises a transistor of a second conductivity type different from the first conductivity type (see Column 21, Lines 5-56).

Should it is shown that Takahara neglects to teach such transistor subject matter with sufficient specificity, the examiner takes official notice that it would have been well within the skill of an artisan at the time of invention to use transistors of different conductivity types to form Takahara's transfer switches, so as to make use of commonly available and readily understood types of electrical switches.

Regarding claim 13, Takahara discloses the first and second transfer switches and the picture signal supply means are disposed on a common substrate with the active matrix substrate (see Figs. 11 & 12; Column 20, Line 24 - Column 21, Line 56 and Column 13, Lines 20-35).

Should it is shown that Takahara neglects to teach such common substrate subject matter with sufficient specificity, the examiner takes official notice that it would have been well within the skill of an artisan at the time of invention to dispose Takahara's first and second transfer switches and the picture signal supply means on a common substrate with the active matrix substrate, so as to make use of commonly available and readily understood types circuitry manufacturing techniques.

Regarding claim 15, Takahara discloses the active matrix substrate comprises a single crystal substrate (see Column 9, Line 10 - Column 13, Line 65).

Should it is shown that Takahara neglects to teach such single crystal subject matter with sufficient specificity, the examiner takes official notice that it would have been well within the skill of an artisan at the time of invention to use a single crystal substrate as Takahara's active

matrix substrate, so as to make use of a commonly available and readily understood type of substrate.

Response to Arguments

22. Applicant's arguments filed 28 January 2008 have been fully considered but they are not persuasive.

The Applicant contends, "*independent Claims 8 and 9 have been amended so that the invention may now be characterized as having first and second transfer switches for connecting a (certain one) signal line. The Office Action [mailed 12 March 2007] asserts that the second transfer switch of the present invention corresponds to TFT of the Hiroki patent. In this regard, a switch in a sampling and buffer circuit 130 connected to a signal line (1) is connected to a first analog video signal (line) 129, but TFT is not connected to a second analog video signal (line) 130. Accordingly, TFT of the Hiroki disclosure is in no way analogous to the second transfer switch in the present invention, so that it is believed that the Hiroki patent is deficient as a rejecting reference*" (see Page 7 of the Amendment filed 28 January 2008).

However, the examiner respectfully disagrees. Hiroki teaches a first transfer switch [Fig. 8A; positive-signal controlled leftmost CMOS circuit within the 'Sampling Circuit and Buffer Circuit'] for connecting (electrically) a signal line [Fig. 8A; Signal Line(1)] with a first common signal line [Fig. 8A; horizontal signal line segment output from 27] for selectively supplying the picture signals of one polarity [e.g., positive polarity] to the signal line, and

a second transfer switch [Fig. 8A; negative-signal controlled leftmost CMOS circuit within the 'Sampling Circuit and Buffer Circuit'] for connecting (electrically) the signal line [Fig. 8A; Signal Line(1)] with a second common signal line [Fig. 8A; the vertical signal line segments between the transfer switches and the horizontal signal line segment output from 27] for selectively supplying the picture signals of other polarity [e.g., negative polarity] to the signal line, wherein the signal line is connected to the first transfer switch and the second transfer switch (see Fig. 8A; Column 3, Line 4 -Column 4, Line 65)

Applicant's arguments with respect to claims 8-15 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed proper, necessary, and thereby maintained at this time.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
23 April 2008